DARPA workshop presentation, 10/12/2021

Electronics for dense, efficient G-band arrays

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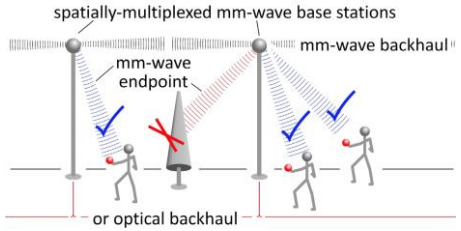
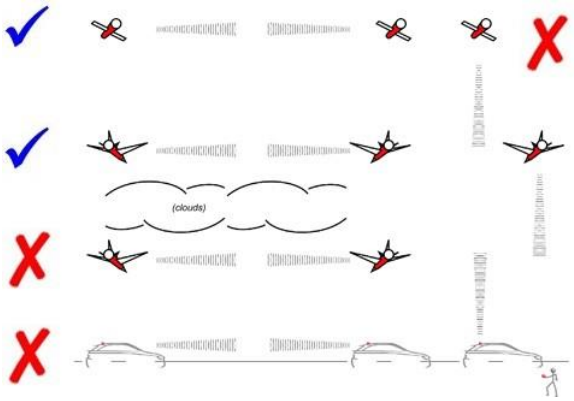
100-300GHz wireless: applications

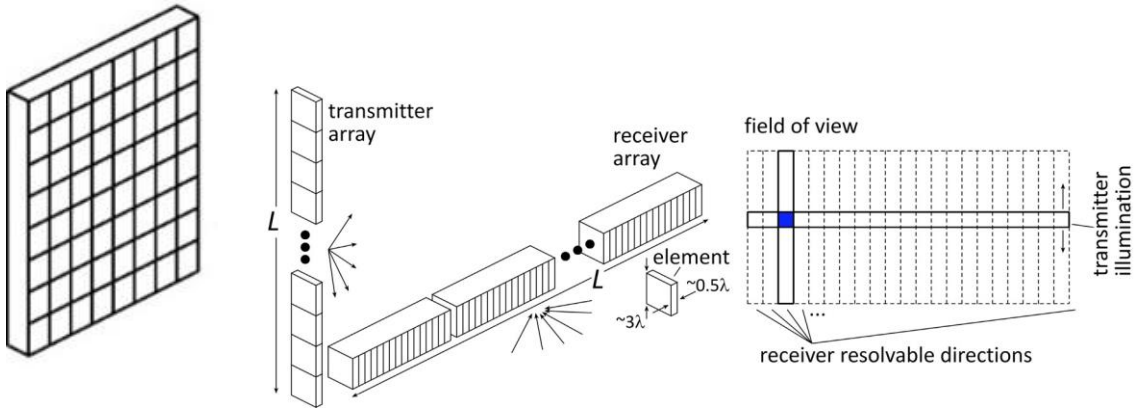
Short-range high-capacity wireless links
(civilian infrastructure)



~300m range high-resolution imaging radar
concealed weapons detection
cars/drones in poor-visibility weather

Long-range, high-altitude links
satellite-satellite, or air-satellite





The 100-300GHz 2D Array Challenge

Arrays can be made from either **tiles** or **trays**

Arrays might be vast: 100-1,000-10,000 elements

Arrays must be dense:

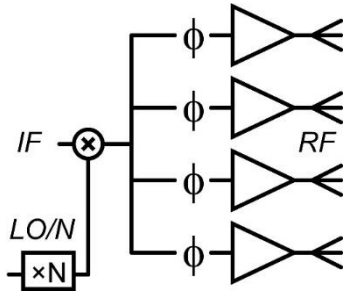
Many DC/IF/LO lines, plus antenna interface.
Fitting IC functions into available area.
Removing the heat.

IC density :

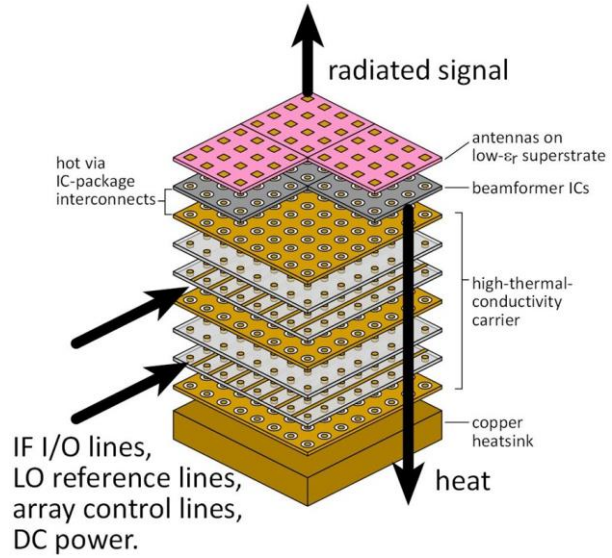
must fit PA, phase-shifter in ~$(0.5\lambda)^2$.
0.68mm × 0.68 mm @ 220GHz.

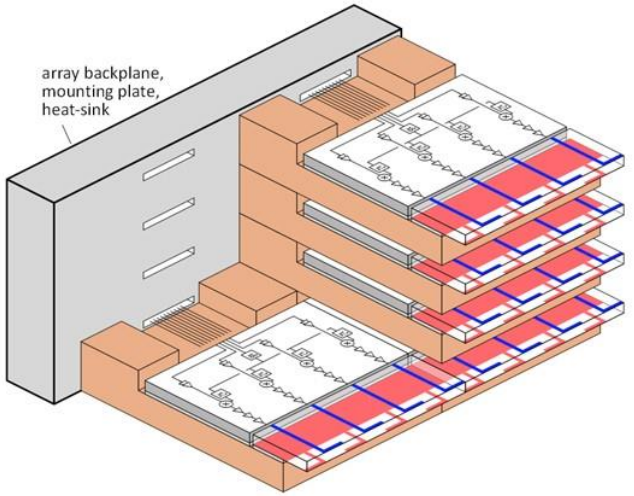
Power and efficiency :

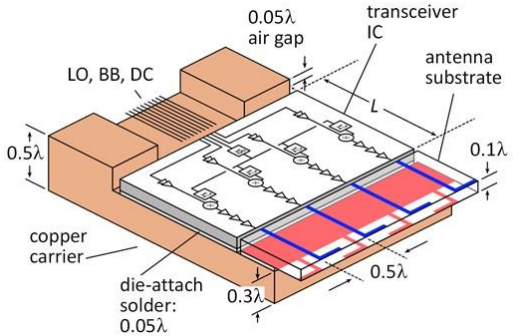
high thermal load
high-efficiency PA at target (~200mW) power



f	100	150	200	220	250	GHz
λ	3	2	1.5	1.36	1.2	mm
λ/2	1.5	1	0.75	0.68	0.6	mm

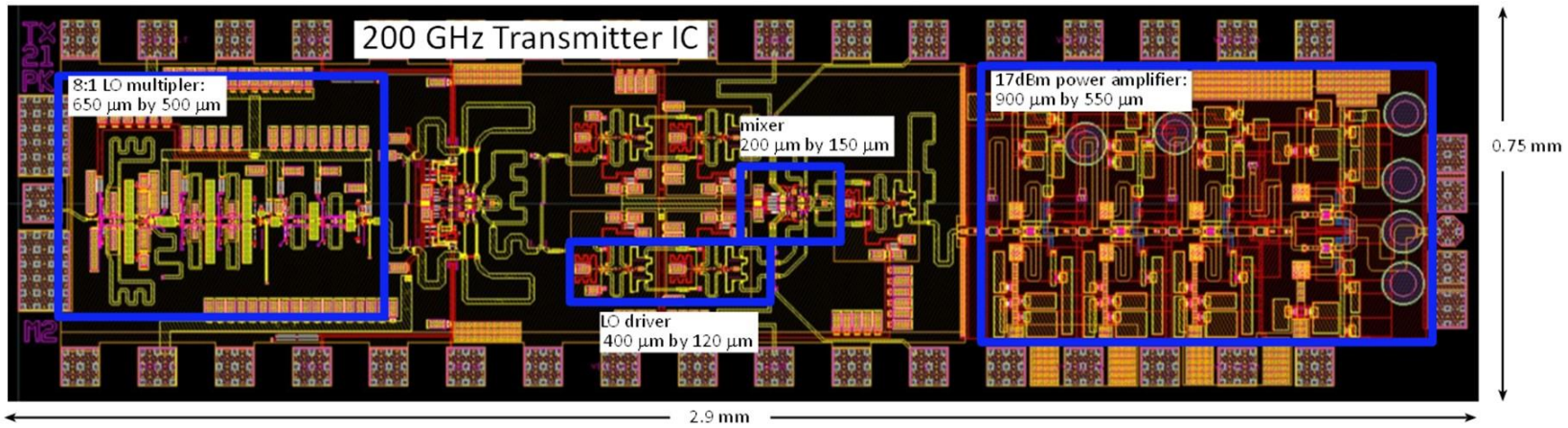


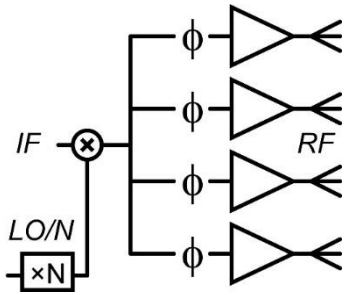




A simple 200GHz, 0.6λ×0.6λ array can just fit

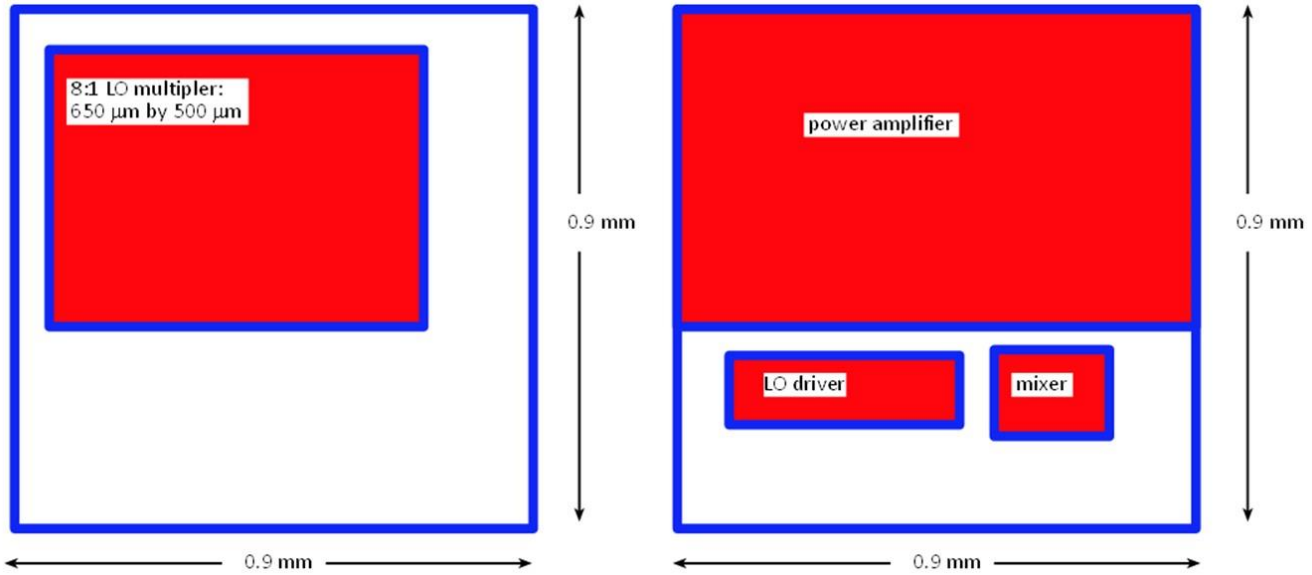
Seo et al, 2021 IMS

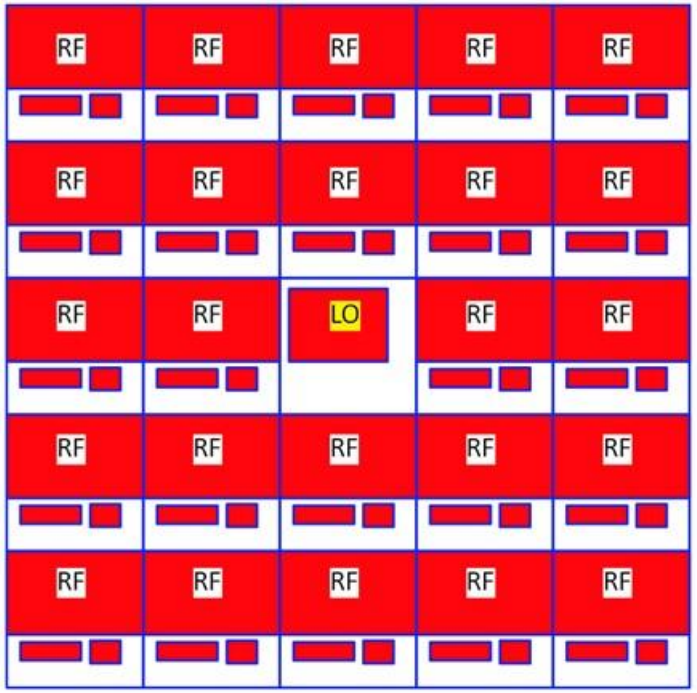




24-element array

4.5mm × 4.5mm



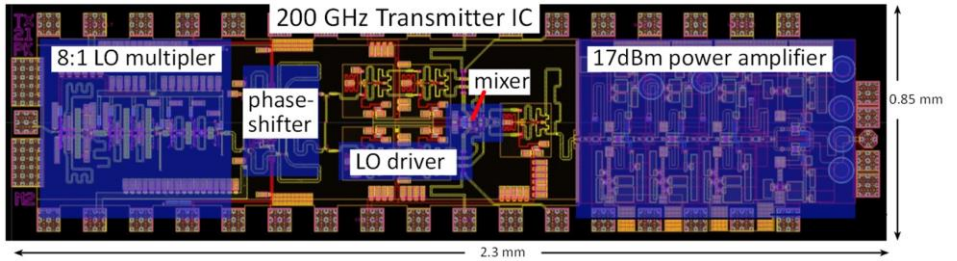


Will a 220GHz dual-pol T/R array fit in 0.5λ×0.5λ ?

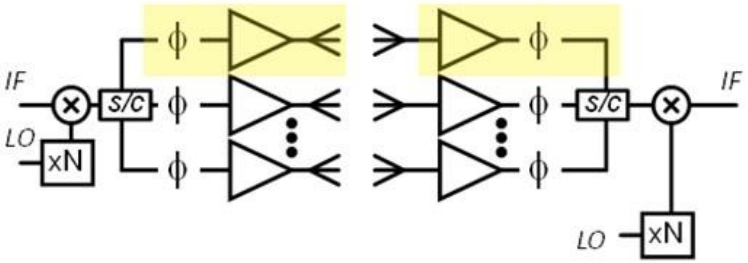
Substantially denser integration is needed.

All blocks must get smaller

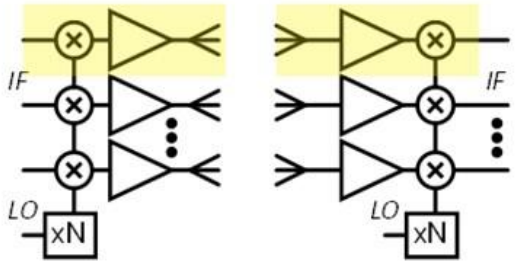
PA must get considerably smaller (seek 200mW, not 50mW)



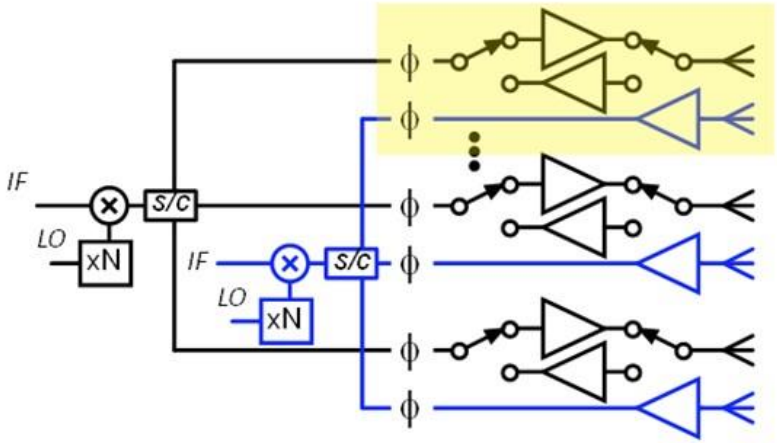
Single-beam transmitter and receiver



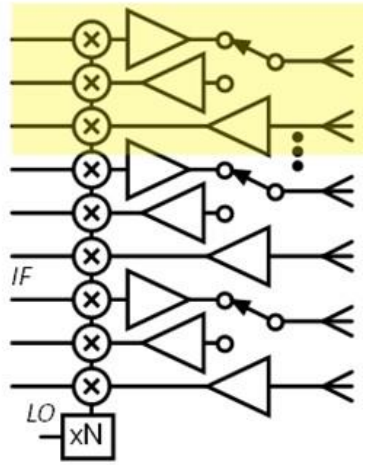
Multi-beam transmitter and receiver



Single-beam dual-pol receiver+ transmitter



Multi-beam dual-pol receiver+ transmitter



Must increase IC density

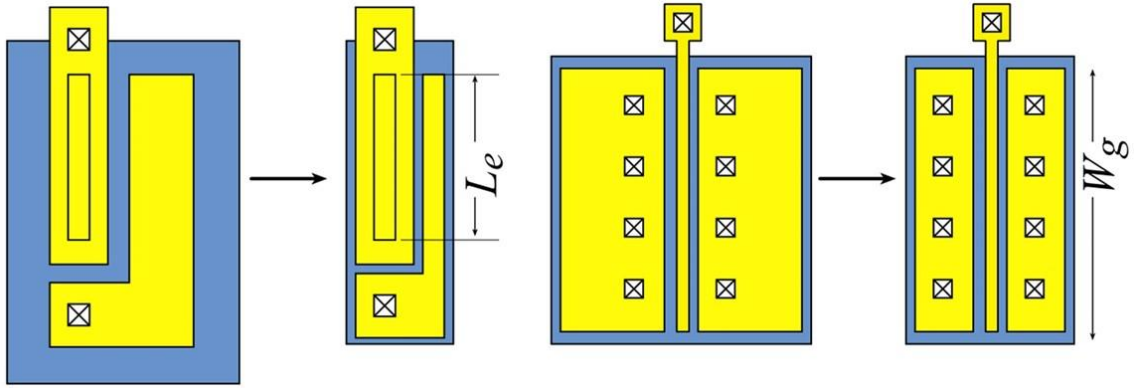
Unlike CMOS, other mm-wave technologies are optimized for speed, not density

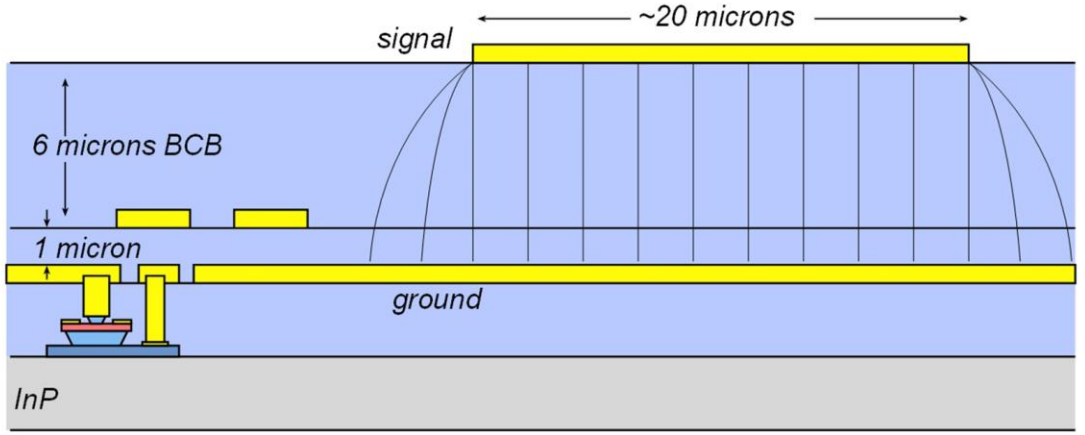
Transistors have been scaled for speed, but not always for density

FETs: small gate length, small gate-source, gate-drain spacings: fast
FETs: often large S/D pitch: low density
HBTs: small emitter widths, small base-collector junction widths: fast
HBTs: often large collector contacts and collector mesa: low density

Interconnects have been sized for low-loss 25-75Ω lines, but not always for density

wide for desired 25-75Ω Zo, low loss.
wide for high current-carrying (PAs)





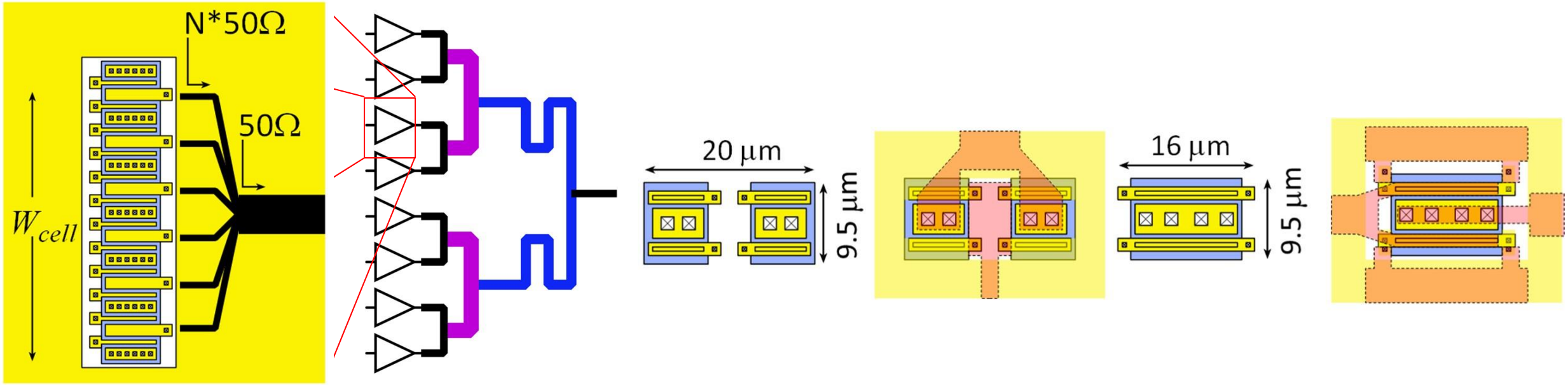
PAs need fine-pitch interconnects: size, PAE

Allows dense multi-finger transistors

Within-cell wires are short: small parasitic inductances, capacitances

Because local impedances are high, capacitance is the main problem; **narrower is better**.

Don't want 50Ω lines within multi-finger power transistor cell.



All transceiver blocks need fine-pitch interconnects

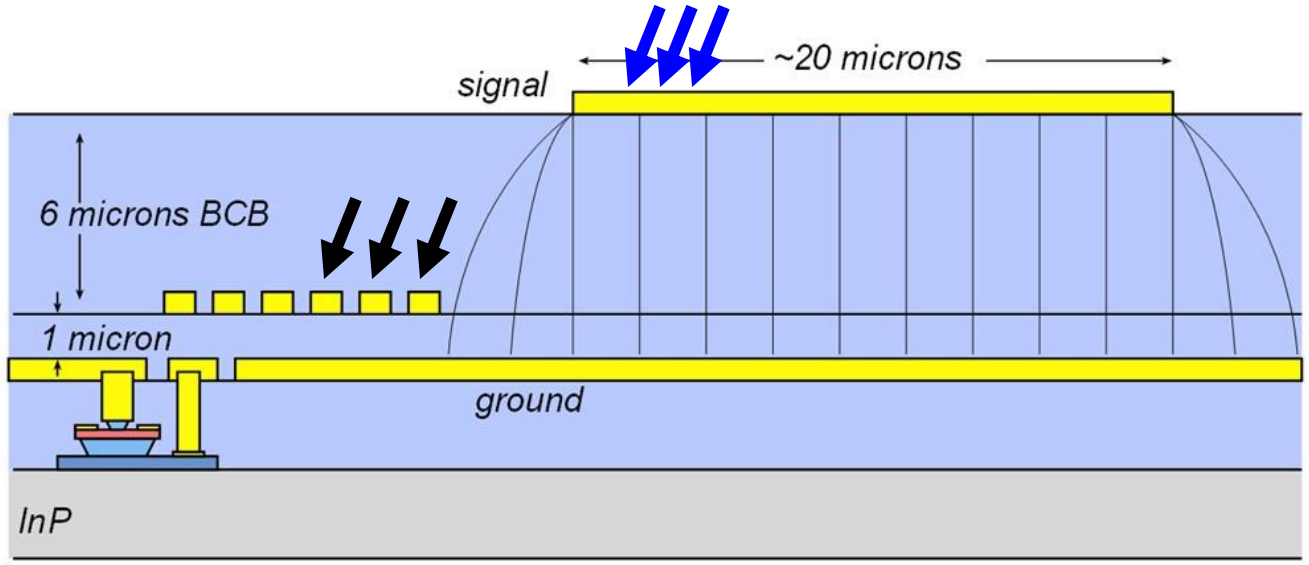
LO frequency multipliers, phase-shifters, LNAs, mixers, driver amplifiers

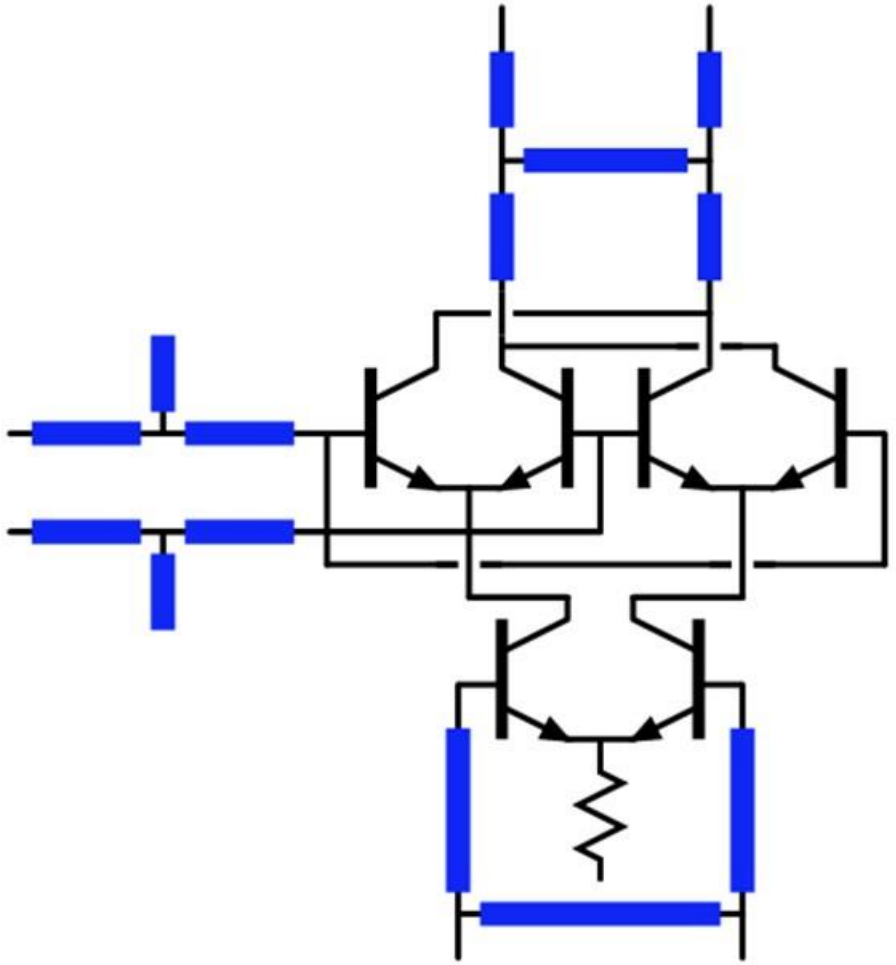
Controlled-impedance interconnects, and matching, between blocks

→ wide, lower-density interconnect

Short, random-impedance wires within blocks.

need fine-pitch wiring, small-footprint transistors
small inductive, capacitive wiring parasitics
wires need not be 50Ω→ narrow→ compact





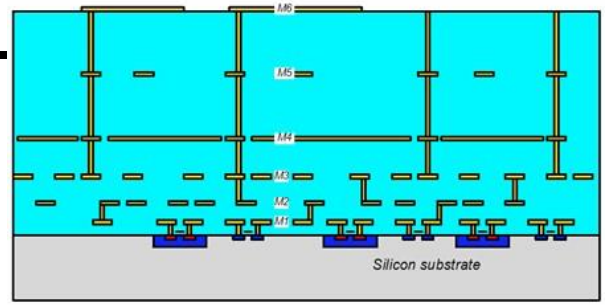
Fine-pitched interconnects

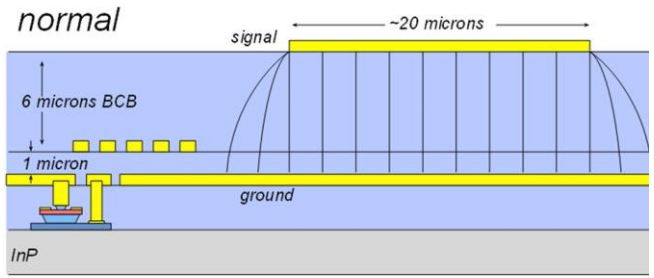
CMOS and SiGe: interconnects above IC
- lower planes: **dense**, random impedance
- upper planes: **sparse**, controlled-impedance.

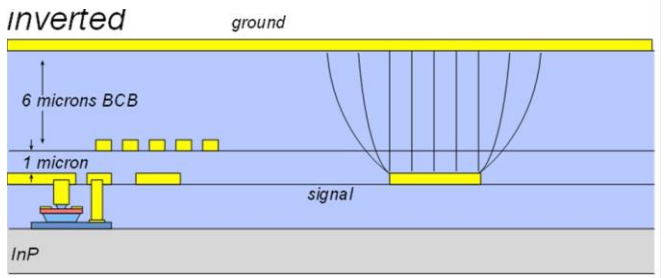
InP HBT: interconnects above IC
- upper planes: **sparse**, controlled-impedance.
- need to add **dense** interconnect layers
- normal or inverted microstrip

Most mm-wave GaN : ground below IC, signal above IC
- substrate microstrip.
- lower-**density** interconnects.
- minimum ground via spacings.

GaN with CMOS/InP-like wiring for denser interconnects ?
- dielectric loading → increased C_{gs}, C_{gd} → decreased f_τ , f_{max} ✗
- substantial effect with FETs: (small g_m/W_g, small C/W_g)
- minor effect with BJTs: (large g_m/W_g, small C/W_g)
- **Possible solution ?** Air cavity above transistors







Need denser bypass capacitors

Not for small-value impedance-matching capacitors

high C/A → small dimensions→ large capacitance variability given normal linewidth variations

Application: RF bypass capacitors

goal: compact IC layouts, compact multi-finger power transistor cells

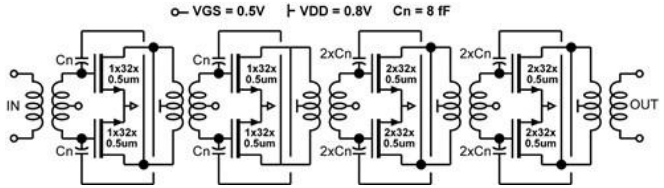
goal: avoid LC self-resonance. Need >>220GHz (class A), >>440GHz (class B)

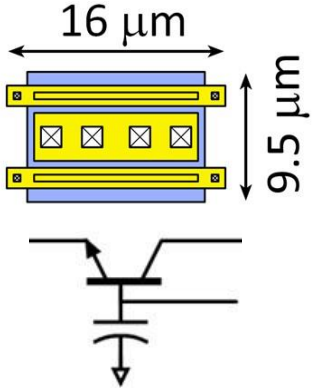
Application: supply bypass capacitors

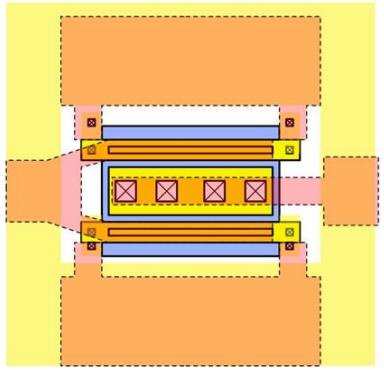
smaller bypass capacitors; with good bypassing, don't need differential stages for supply-related stability

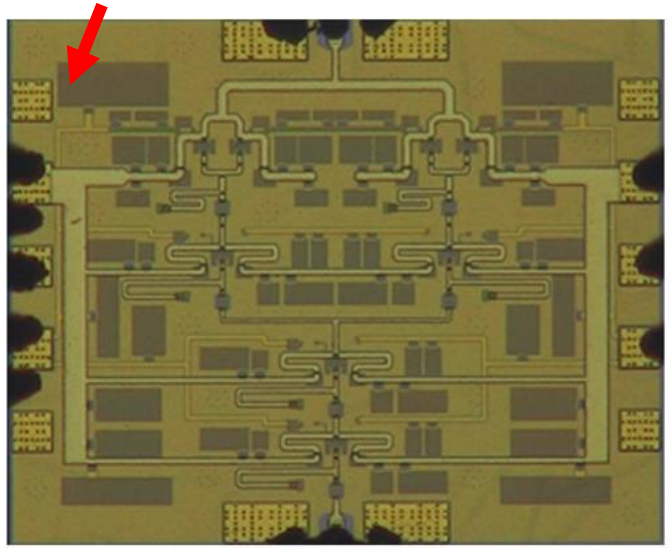
Potential approach: replace 200nm Si_xN_y with ~20nm ZrO_2.

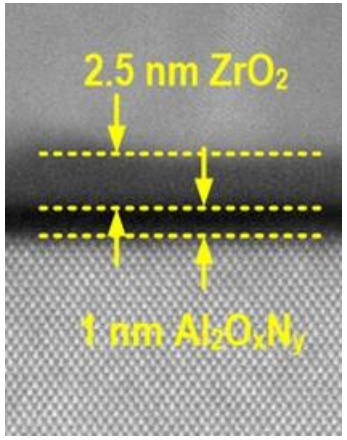
~35:1 smaller area for same capacitance

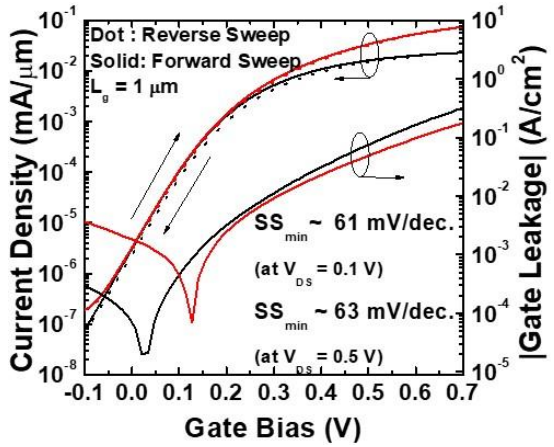












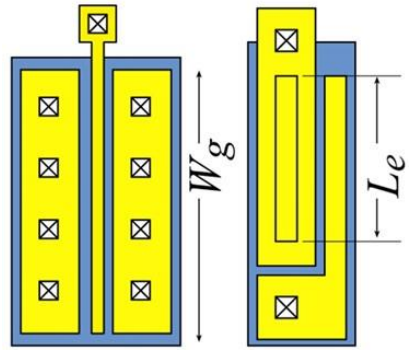
What sets DC power in mmWave ICs ?

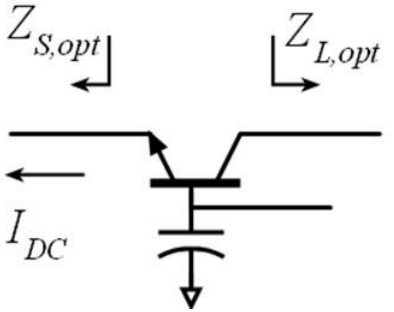
$P_{DC} = V_{DC} \times I_{DC}$
Transistor is sized appropriately for the selected I_{DC}.
What size, what I_{DC} do we pick ?

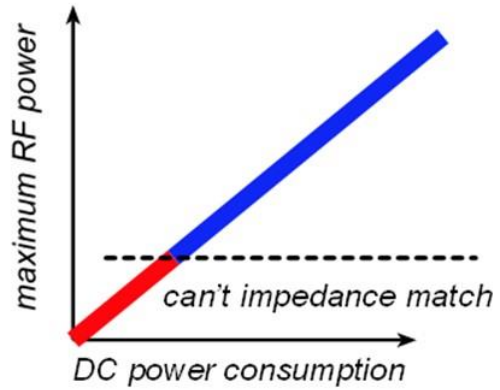
Expected: device size, P_{DC} proportional to maximum RF output power
class-A PAs: $P_{RF} = (1/2)P_{DC}$.
Less required RF power→ less consumed DC power
Yet, we often cannot obtain this.

Impedance-matching sets minimum device size, minimum DC power
small-signal stages: optimum Z_s, Z_L tend to be proportional to $(1/g_m)$
small I_{DC}→small g_m→large optimum impedances, can't match !

Bipolar (SiGe, InP) transistors are attractive for low-power mmwave ICs
high g_m/I_{DC} ratio, ~10:1 better than FETs.
high g_m per unit finger length; small transistor footprint







Efficient, small 220GHz PA: what do we need ?

Compact multi-finger transistor layouts

Efficient, compact on-wafer power-combining

Good transistor models: comprehensive measurements

Good power measurements calibrated to the IC pads

Load-pull measurements :

At 220GHz ?

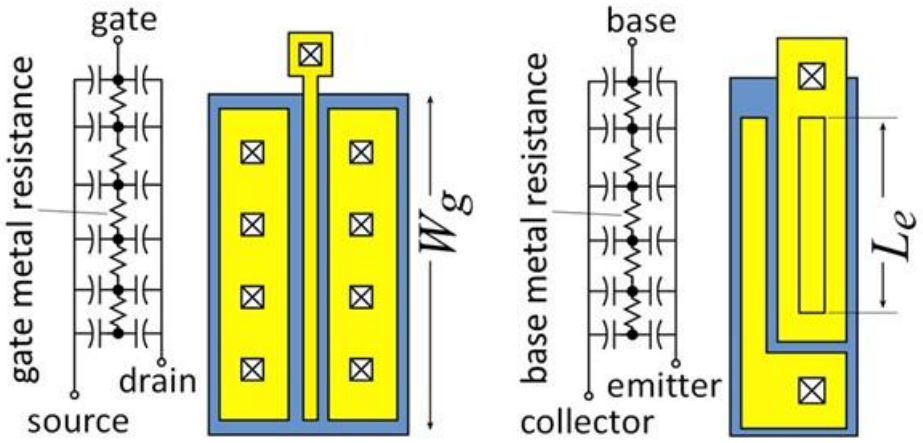
Extrapolated from 94GHz ?

Current density, finger pitch limit cell output power

Electrode RC charging time $\propto$ (finger length)^2

Maximum finger length $\propto 1/\sqrt{\text{frequency}}$

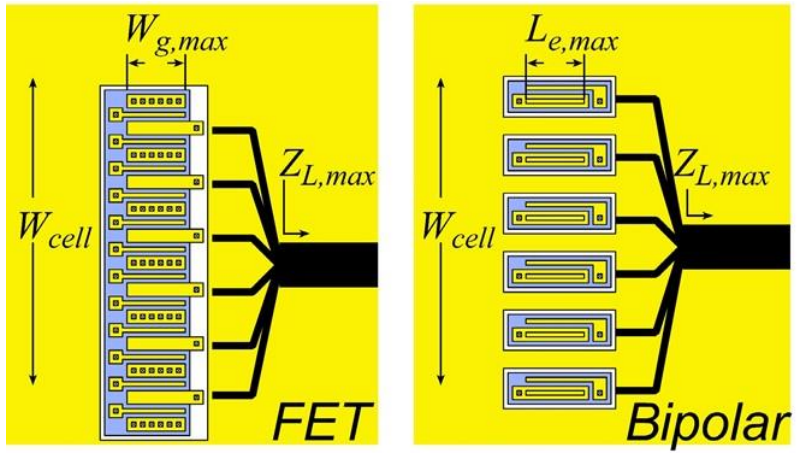
Current per finger $\propto 1/\sqrt{\text{frequency}}$



Maximum cell width $\propto 1/\text{frequency}$

Maximum number fingers $\propto 1/\text{frequency}$

Maximum current per cell $\propto 1/\text{frequency}^{3/2}$



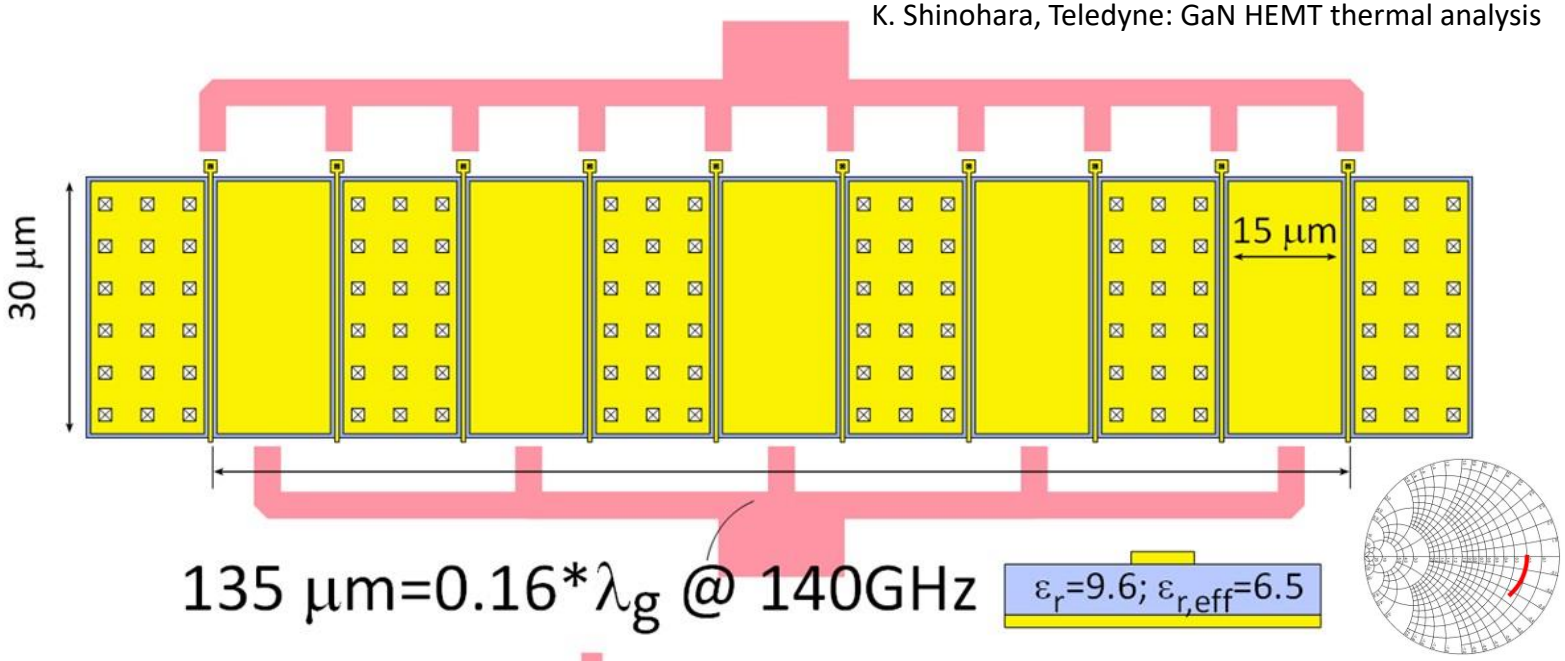
Maximum RF power per cell $\propto$ (maximum load resistance) $\cdot$ (maximum current)^2 $\propto 1/$(frequency)^3

Compare to Johnson F.O.M.: maximum power per cell $\propto$ (maximum voltage)^2 / (minimum load resistance) $\propto 1/$(frequency)^2

Current density, finger pitch limit cell output power

K. Shinohara, Teledyne: GaN HEMT thermal analysis

50Ω GaN PA cell @ 140GHz (1.6W)
25V swing, 1.67mA/μm,
gates: 30 μm width, 15 μm pitch

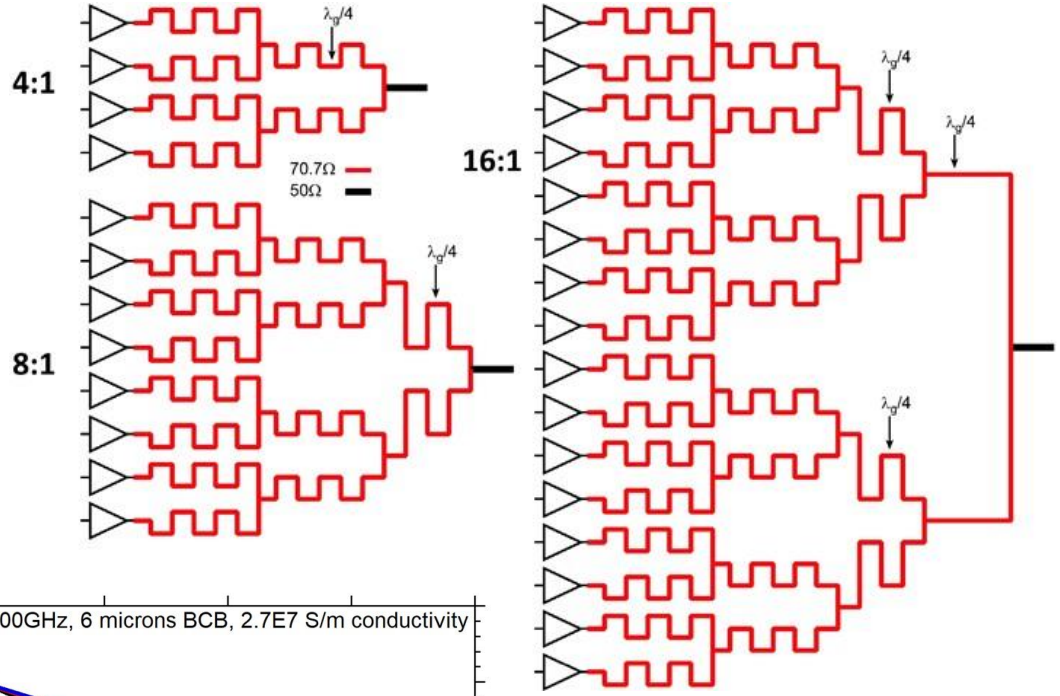


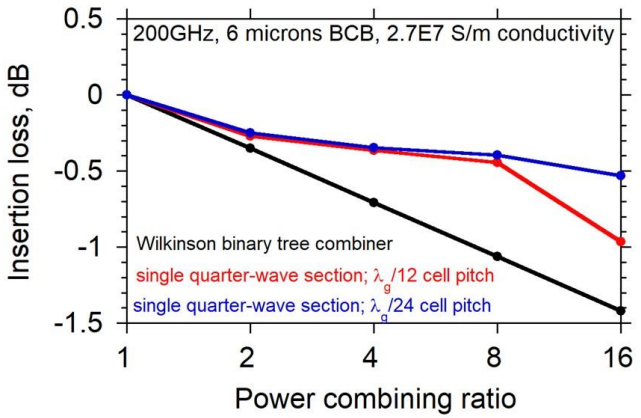
50Ω InP HBT PA cell @ 280GHz (40mW)
4V swing, 3.3mA/μm,
emitters: 6 μm length, 6 μm pitch

High V_{br}, low I_{max} ? Device sized to drive 50Ω might approach $\lambda_g/4$ width.
Small finger pitch is critical; limited by thermal design

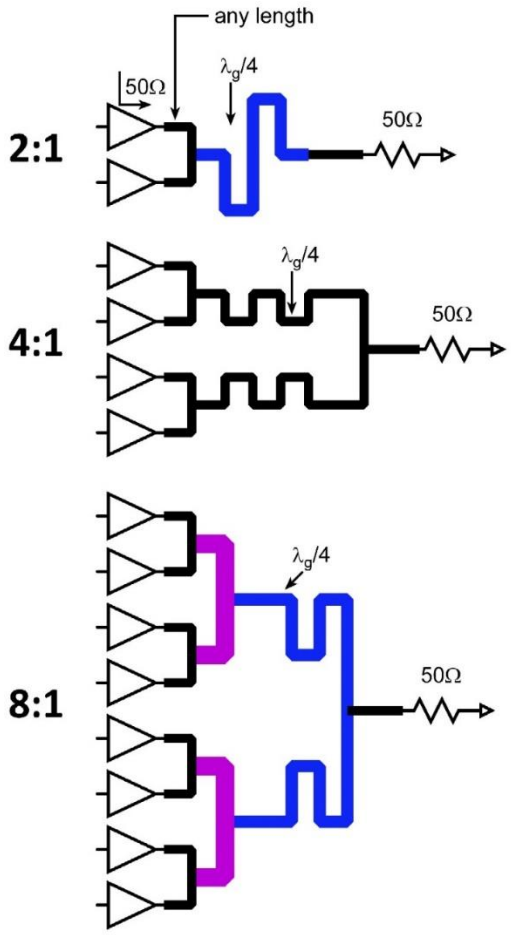
Lower-loss corporate power-combiners

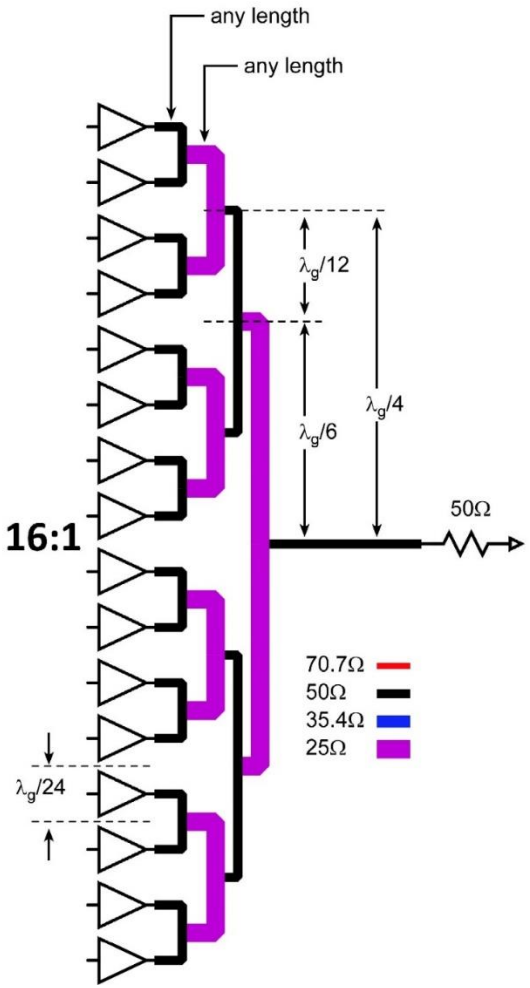
Wilkinson trees are lossy:
Signal passes through *many* 70.7Ω, λ/4 lines.
λ/4 lines are long.
70.7Ω lines are narrow…and lossy→ High loss.





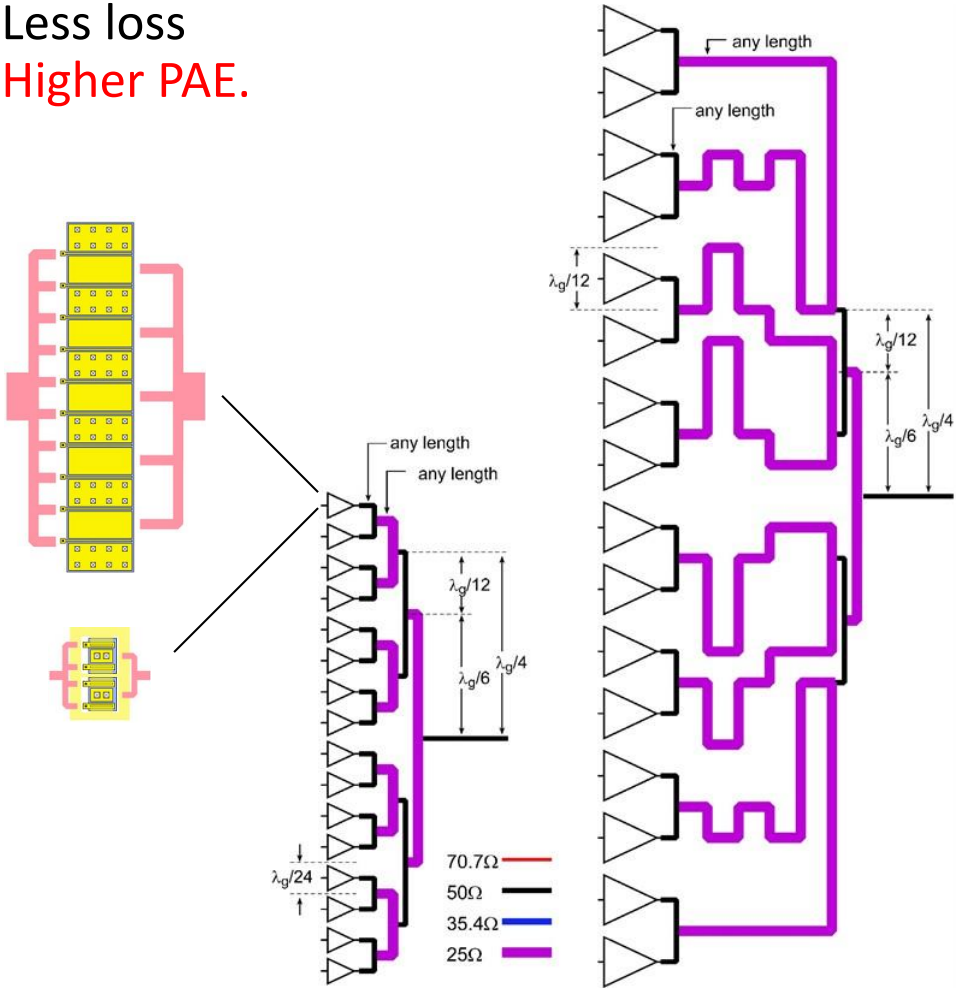
Single-(λ/4) combiners are much less lossy
Each design uses a single *effective* λ/4 section.
Shorter lines, low-Z_o lines → lower loss
But, low loss only if transistor cells fit.



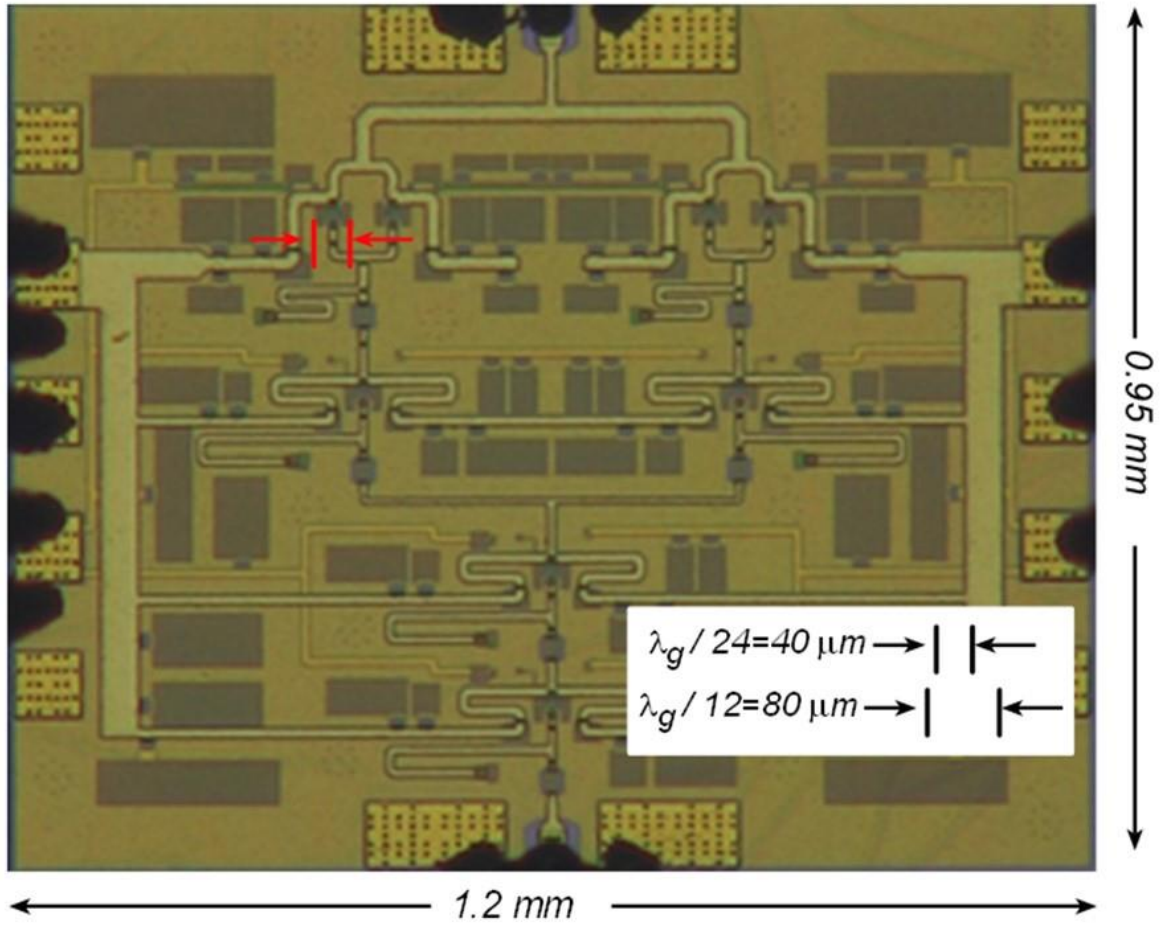


Denser interconnects: improved PAE

Dense wiring: short lines: low loss
Smaller wiring pitch & capacitors
Smaller multi-finger footprint,
Shorter combiner lines
Less loss
Higher PAE.



Present vs. desired IC density
$\lambda_g/24$ cell pitch: much smaller than in present ICs.
Need: smaller wiring pitch & capacitors, better heat removal.
Some matching elements hard to fit: challenging layout.



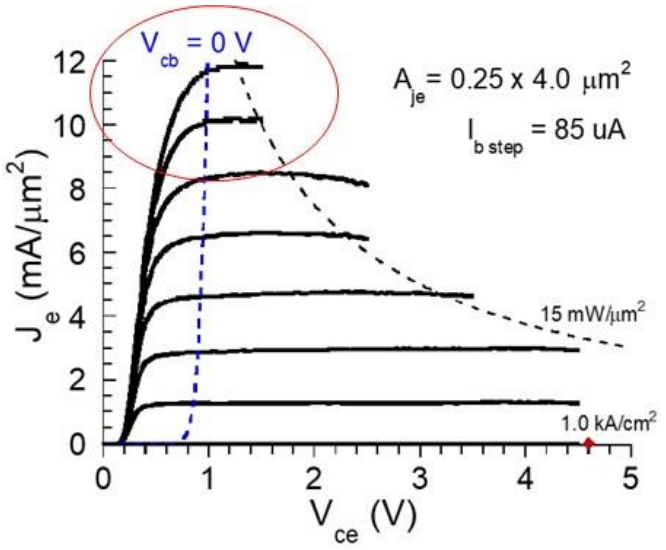
Need accurate transistor models over full loadline

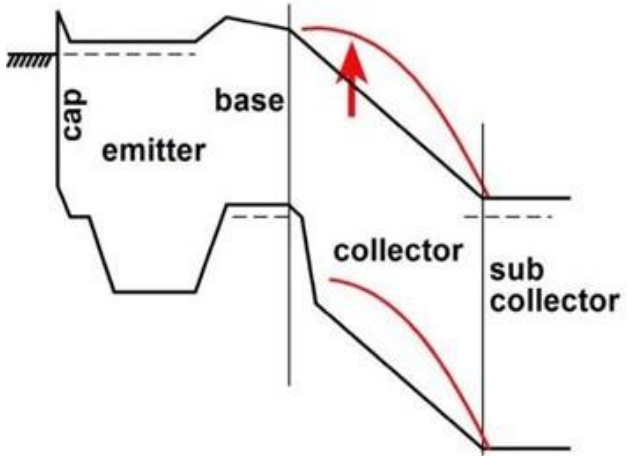
Observation: PA simulations strongly affected by details of saturation model
Static saturation (I-V collapse): higher simulated PAE
Dynamic saturation in BJT's: (Kirk effect: increased C_{cb} and increased τ_c): lower simulated PAE
Dynamic saturation in FETs: (back-injection: increased C_{gd} and increased τ_{ch}): lower simulated PAE

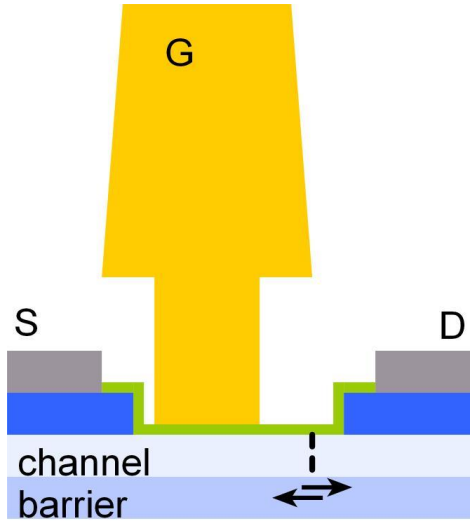
Implication: PA design needs accurate models over full signal swing.

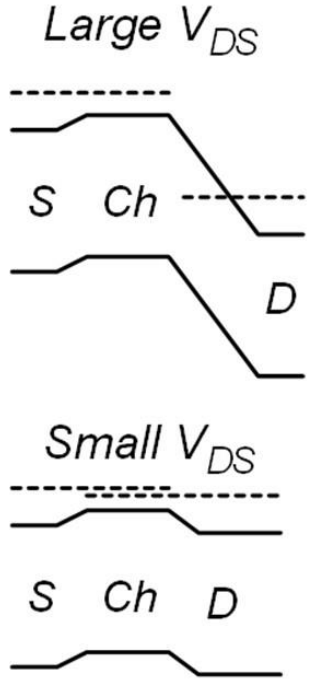
Also: transit time and capacitance variations over (I,V) plane

Prescription: Develop accurate model over entire PA loadline
Over (I,V) plane: (a) measure S-parameters, (b) extract model at each bias point
Fit to large-signal model over entire transistor safe operating area.









Extrapolate W-band load pull to 220GHz ?

Why not make W-band load-pull measurements, use these for 220GHz design ?

Large-signal effects, particularly saturation, can be static, dynamic, or both.

Example: HBT low-voltage limit, aka Kirk effect.

Decreased I_c, increased τ_c, increased C_{cb}.
All reduce the PA gain, all reduce the output power.
Can load pull tell you how much of each ?
Strong frequency variation of dynamic effects (τ_c, C_{cb})
No frequency variation of static effects (I_c)

FETs in saturation: similar mix of static, dynamic effects.

Extrapolating load-pull data to higher frequencies can thus be ambiguous.

Must model device self-heating

Observation: Good PA modeling at low V_{cc}, weaker modeling at high V_{cc}.

Inaccurate device model ? Unlikely: extensive characterization at foundry

More likely: transistor and IC self-heating

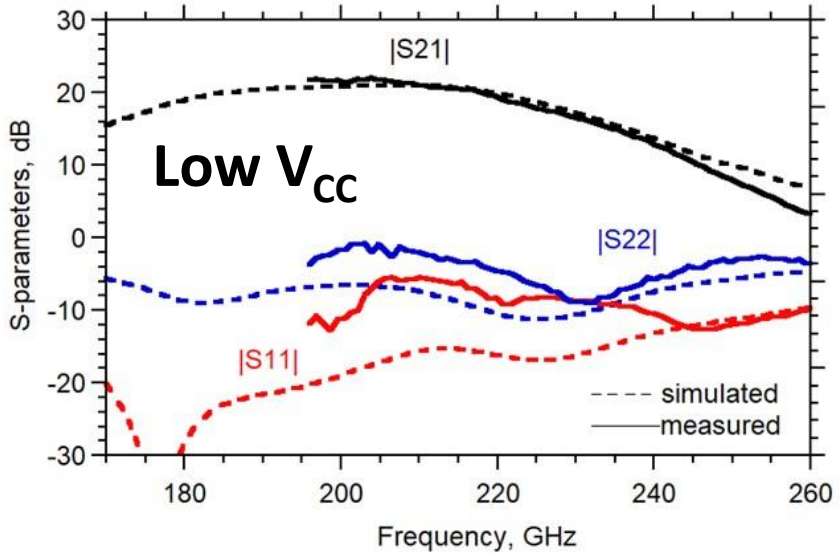
Need accurate temperature-dependent transistor electrical model

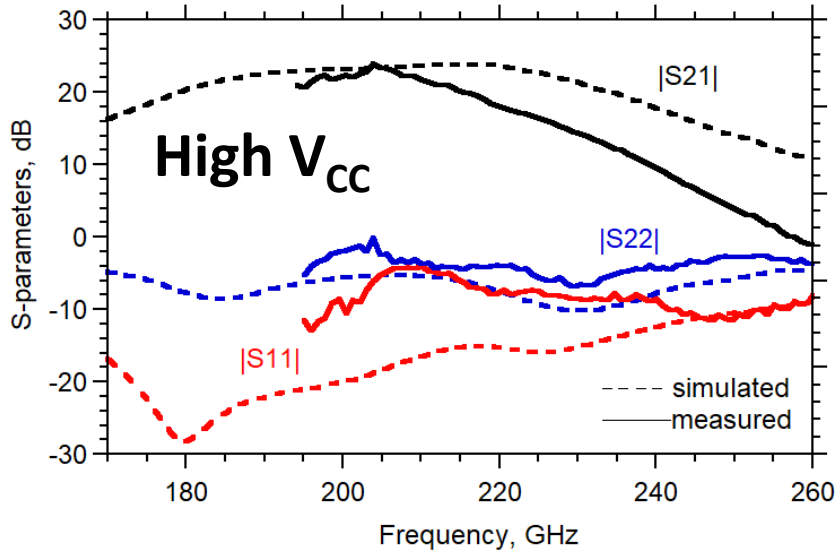
Need accurate model of device/IC self-heating

Dense IC: need good thermal management.

HBT self-heating observation

FETs show similar behavior





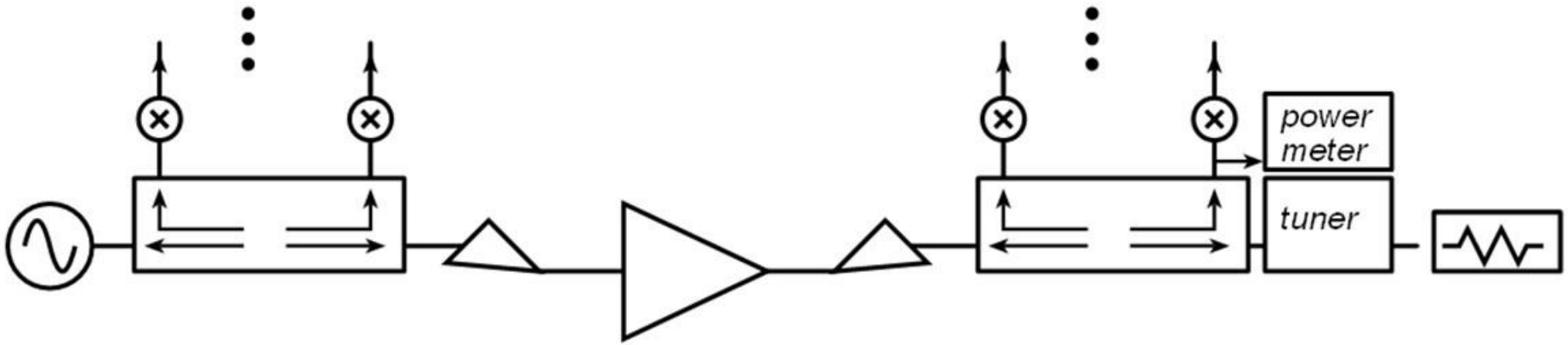
Power measurements calibrated to the IC pads

Present 220GHz PA characterization: scalar power correction

Output power measured using meter and waveguide-coupled wafer probe.
Probe loss corrected by 2-probe though-line measurement.
Does not correct for (S_{11}, S_{22}) of probe or power meter.
Does not ensure that PA load impedance is 50Ω (damaged/worn probe).

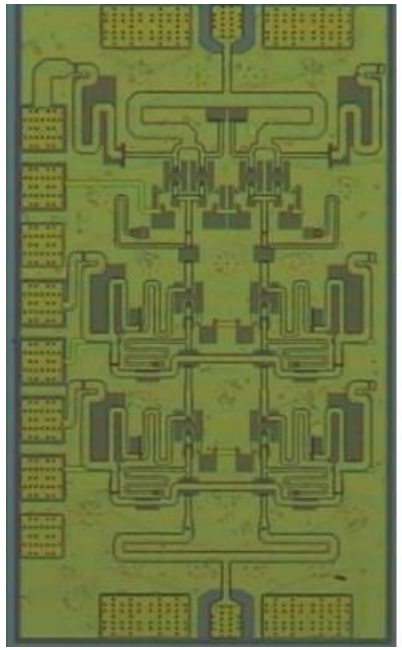
Alternative: power meter integrated with network-analyzer

NWA calibration moves reference plane to IC probe pad
Load impedance can be determined
Adding E/H tuner: limited tuning of load impedance

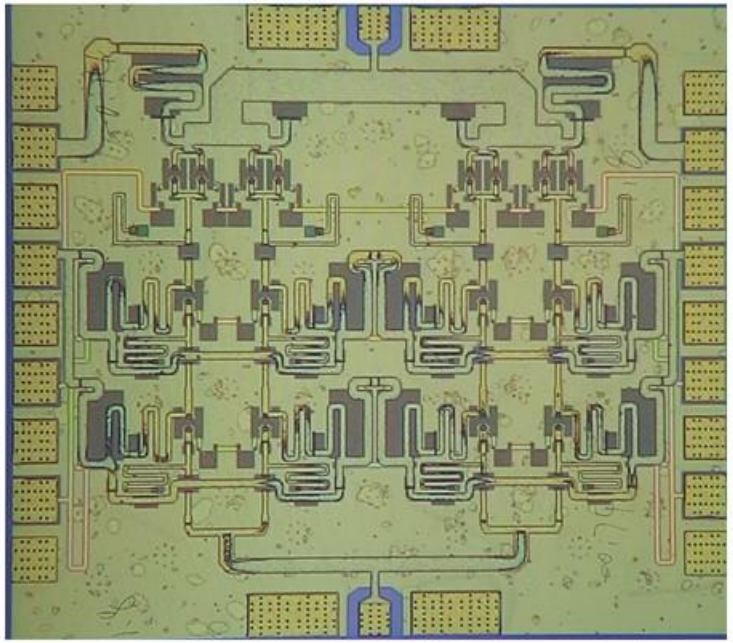


Recent high-efficiency 100-300GHz PAs

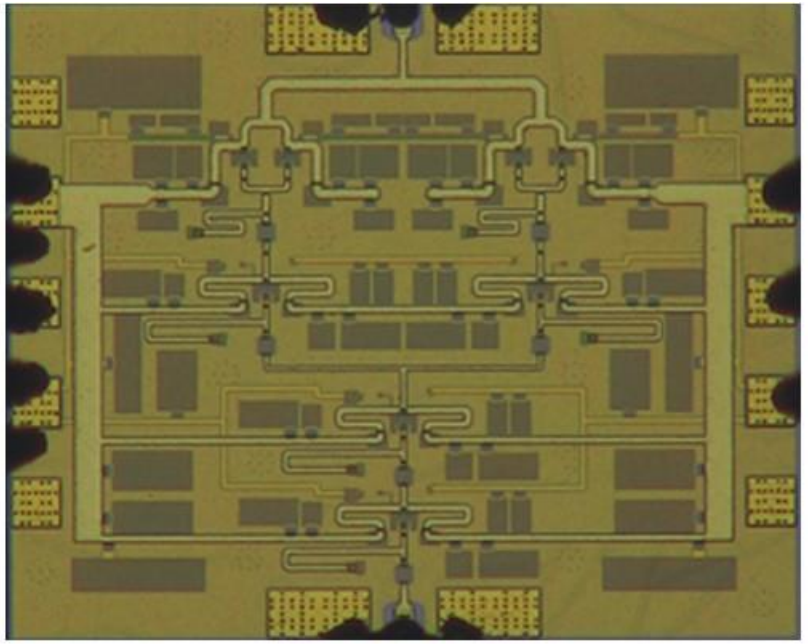
Ahmed et al, 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC
Teledyne 250nm InP HBT technology



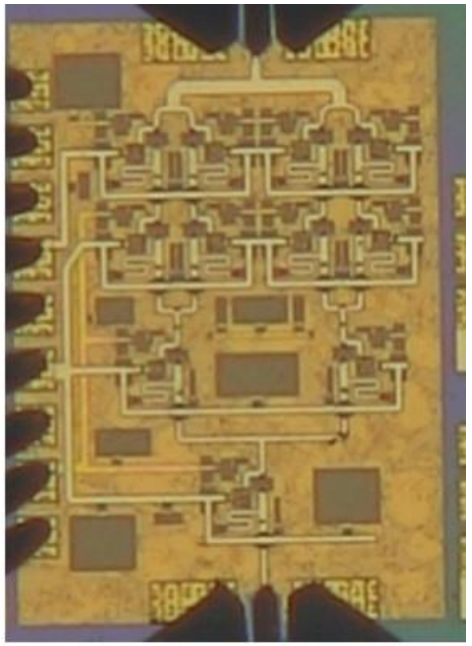
140GHz, 20.5dBm, 20.8% PAE



130GHz, 200mW, 17.8% PAE



194GHz, 17.4dBm, 8.5% PAE



266GHz, 16.8dBm, 4.0% PAE

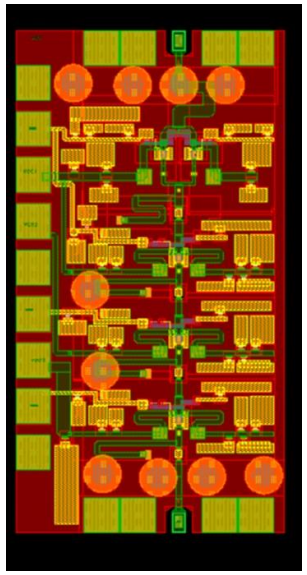
11.3% PAE, 17.0dBm at 190GHz

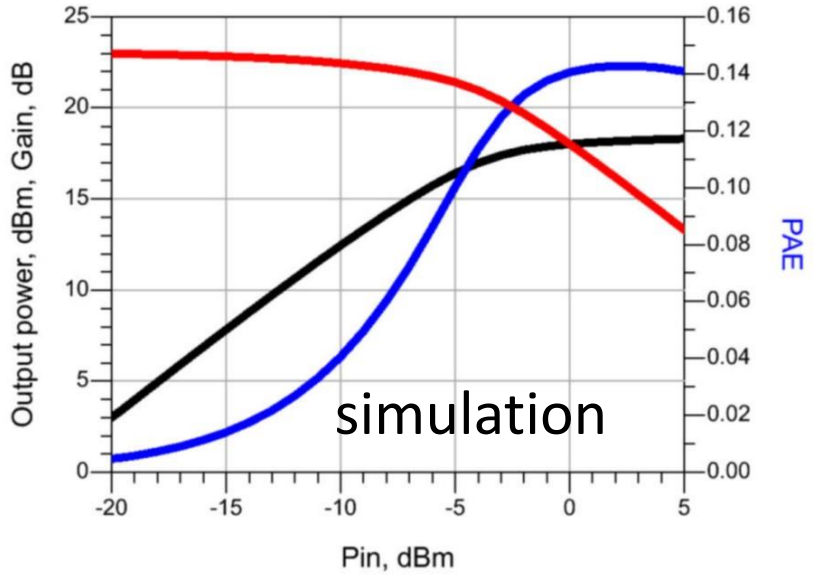
Teledyne 250nm InP HBT technology

Ahmed et al, unpublished

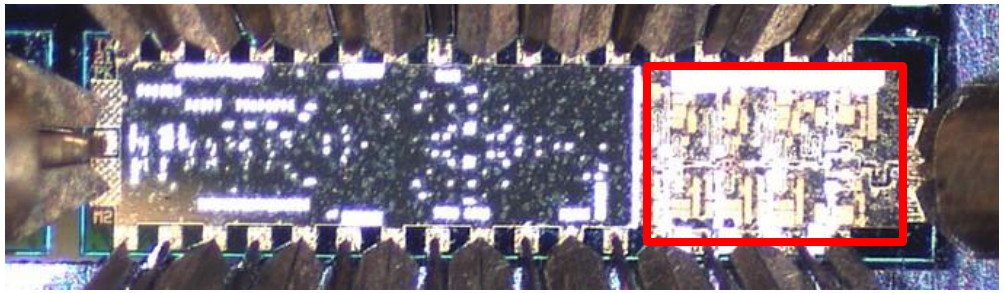
Simulated:
14% PAE, 17.5dBm at 210GHz

Measured:
11.3% PAE, 17.0dBm at 190GHz

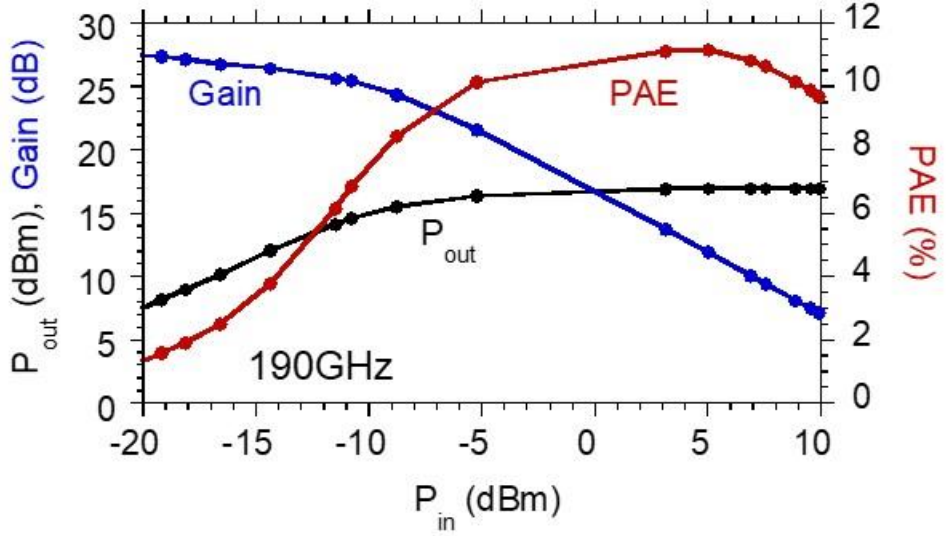




(Used in 190-210GHz transmitter IC)



M. Seo et al, 2021 IMS



Feasibility of 220GHz, 200mW PA with 30% PAE

Design using TSC 250nm InP HBT model

2-stage, 22dB gain at saturation

transmission-line loss models fit to measurements.

→ 22% PAE at 200mW output power.

Approaches to reach 30% PAE.

Slightly adjusted transistor epi material.

Class B design.

end